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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/546,620	08/23/2005	Takashi Kariya	276730US90PCT	4465

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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
12/14/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/546,620	KARIYA ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/20/09*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-4,6-8,11-12,18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8,11,12 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/30/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. (cited in the record) in view of Jones et al. (U.S. Patent 5,541,450).

As to claim 1, Sakamoto et al. discloses a multi-layer printed wiring board as shown in figure 1 comprising:

a first substrate (12, 11b) having an opening (15) and a plurality of terminals (pads or wirings/lands on top surface of substrate 12, 11b),

a second substrate (11a, 12) laminated to the first substrate (12, 11b) having a plurality of terminals (the pads or lands on a bottom surface of the substrate 12) and having a metallic layer portion (electrodes 22) positioned in the opening (15) of the first substrate (12, 11b), and a plurality of non-through holes (see figure 1) filled with conductive materials (14) and electrically connected to the metallic layer portion (22), a carrier board (16) having terminals (21) formed in the opening and connected to the metallic layer portion (22) of the second substrate (11a).

Sakamoto does not specific disclose an IC formed in the opening having terminals opposite side of the metallic layer such that the metallic layer and non-through holes of the second substrate being irradiate heat generated by the IC component.

Jones shows a BGA semiconductor package (30) as shown in figure 2 comprising a first substrate (31) having an opening (33) loaded with an IC (18) having terminals (22) formed on top surface of the IC (18), the IC (18) formed on a metallic layer portion (36, see column 3, line 34).

It would have been obvious to one having ordinary skill in the art at the time was made to have a teaching of Jones employed in the wiring board of Sakamoto et al. in order to form a multi-electronic/chip package.

Regarding claims 3-4, Sakamoto et al. as modified by Jones discloses in figure 1 that the external terminals of the first substrate (12, 11b) disposed offset the external terminals of the second substrate (11a), the first substrate having a plurality of conductive non-through holes (14) connected to the external terminals (top surface of layer 12) and the second substrate having a plurality of conductive non-through holes (14) connected to the external terminals of the second substrate (bottom surface of the bottom layer 12), the conductive non through holes (14) of the first and second substrates are offset each other, see figure 1.

Regarding claims 7-8, 11, Sakamoto et al. as modified by Jones discloses a plurality of bonding pads (37) capable of being rectangular shape of the first substrate provided for the IC (18) having wire bond (44) connected on the pads (37) and the through holes (39) formed underneath of the pads.

It would have been obvious to one having ordinary skill in the art at the time was made to have a teaching of Jones employed in the wiring board of Sakamoto et al. in order to provide an electrical connection.

Regarding claim 18, Sakamoto et al. as modified by Jones that discloses the terminals of the first substrate (12, 11b) are position in a peripheral form surrounding the IC component, and the terminals (14) of the second substrate (11a, 12) are position in a grid form (LGA).

Regarding claims 19-20, Sakamoto as modified by Jones that discloses the IC component (18) has a bottom portion of which an entire surface of the bottom portion of the IC component is loaded over the metallic layer portion (36) of Jones in the second substrate, and the first substrate (31) has a plurality of terminals (37, 41) positioned to be connected to the plurality of terminals of the IC component (18) by wire-bonded connected, and the external terminals and terminals in the first substrate are positioned to face the opposite side of the metallic layer portion of the second substrate. It would have been obvious to one having ordinary skill in the art at the time was made to have a teaching of Jones employed in the wiring board of Sakamoto et al. in order to form a multi-electronic/chip package.

3. Claims 6, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Jones as applied to claims above, and further in view of Londa (as in record).

Regarding claims 6, 12, Sakamoto et al. as modified by Jones discloses all of the limitation of the claimed invention except for solder bumps formed on the pads of each

of the substrate. Londa teaches a MCM package as shown in figure 2 that comprising solder bump (74, 92) formed on pads of each of the substrate.

It would have been obvious to one having ordinary skill in the art at the time was made to have a teaching of Londa employed in the wiring board of Sakamoto et al. in view of Jones in order to form a BGA package or make an electrical connection.

Response to Arguments

4. Applicant's arguments filed 08/20/09 have been fully considered but they are not persuasive.

Applicant argues:

The Office Action states that "Sakamoto et al. discloses a multi-layer printed wiring board as shown in figure 1 comprising ... a second substrate (1 la, 12) laminated to the first substrate (12, 1 lb) having a plurality of terminals ... and having a metallic layer portion (electrodes 22) positioned in the opening (15) of the first substrate (12, 1 lb), and a plurality of non-through holes (see figure 1) filled with conductive materials (14) and electrically connected to the metallic layer (22), a carrier board (16) having terminals (21) formed in the opening and connected to the metallic layer (22) of the second substrate (11 a)" but "Sakamoto does not specific **[sic]** disclose an IC formed in the opening having terminals opposite side of the metallic layer such that the metallic layer and non-through holes of the second substrate **being [sic]** irradiate heat generated by the IC component." The Office Action concludes that because "Jones shows a BGA semiconductor package (30) as shown in figure 2 comprising a first substrate (31) having an opening (33) loaded with an IC (18) having terminals (22)

formed on top surface of the IC (18), the IC (18) formed on a metallic layer portion ...," "[i]t would have been obvious ... to have a teaching of Jones employed in the wiring board of Sakamoto et al. in order to form a multi-electronic/chip package." However, it is respectfully submitted that Sakamoto et al. and Jones et al. do not teach or suggest "a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion ..., wherein the IC component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component" as recited in amended Claim 1."

Examiner disagrees. The Office action is clear and show the combination of the references meets all the limitations of the claimed invention.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lee Jinhee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.